Reg.No.:												

VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN
[AUTONOMOUS INSTITUTION AFFILIATED TO ANNA UNIVERSITY, CHENNAI]
Elayampalayam – 637 205, Tiruchengode, Namakkal Dt., Tamil Nadu.

Question Paper Code: 70048

M.E. / M.Tech. DEGREE END-SEMESTER EXAMINATIONS – JAN. 2025

Third Semester

VLSI Design

P23VD311 – ASIC DESIGN

(Regulation 2023)

Time: Three Hours | Maximum: 100 Marks

Answer ALL the questions

Knowledge Levels (KL)	K1 – Remembering	K3 – Applying	K5 - Evaluating
	K2 – Understanding	K4 – Analyzing	K6 - Creating

PART – A

(10 x 2 = 20 Marks)

Q. No.	Questions	Marks	KL	CO
1.	Mention the classification of ASICs.	2	K2	CO1
2.	State the difference between channeled gate arrays and channel-less gate arrays.	2	K2	CO1
3.	Define "PREP benchmarks".	2	K2	CO2
4.	Mention the uses of programmable ASIC I/O cells.	2	K2	CO2
5.	Write about routing resources used in ACTEL ACT.	2	K2	CO3
6.	Write some hardware description languages.	2	K2	CO3
7.	Write the Verilog code for the multiplexer (2:1).	2	K2	CO4
8.	What are the various cells used in BST?	2	K2	CO4
9.	Summarize the constraints used in system partitioning.	2	K2	CO5
10.	Give the goals and objectives of floor planning.	2	K2	CO5

PART – B

(5 x 13 = 65 Marks)

Q. No.			Questions	Marks	KL	CO
11.	a)	i.	Draw the ASIC design flow diagram and explain each block.	8	K3	CO1
		ii.	Write short notes on sequential logic cell.	5	K2	CO1
			(OR)			
	b)	i.	Show that an n-channel transistor looks like a resistor for small.	8	K3	CO1
		ii.	Write CMOS design rules.	5	K2	
12.	a)		Demonstrate the different I/O requirements.	13	K2	CO2
			(OR)			
	b)		Explain EEPROM technology and anti-fuse technology.	13	K2	CO2
13.	a)		Explain the interconnect architecture used in Altera MAX 5000, 9000, and Xilinx EPLD.	13	K2	CO3
			(OR)			
	b)		Examine the PLA tools in ASIC design software.	13	K2	CO3
14.	a)		Write VHDL code for the following.			
		i.	1.4:1 multiplexer	4	K3	CO4
		ii.	Ripple carry adder			
		iii.	2:4 Decoder	4		
		iv.	4:2 encoder	5		
			(OR)			
	b)		Using Verilog synthesis, write a script to synthesize 4:16 decoders with enable and three-state output.	13	K3	CO4
15.	a)		How does the KL algorithm help with system partitioning in SOC?	13	K2	CO5
			(OR)			
	b)		Illustrate circuit extraction and DRC.	13	K2	CO5

PART – C

(1 x 15 = 15 Marks)

Q. No.		Questions	Marks	KL	CO
16.	a)	Explain the functionality and features of Xilinx I/O blocks.	15	K2	CO2
		(OR)			
	b)	Illustrate the physical design flow of ASIC construction.	15	K3	CO5